SPECIFICATIONS FOR THE NI PXI-5404

100 MHz Frequency Source

Contents

The following conditions apply to these specifications:

- These specifications are valid from 0 °C to 50 °C unless otherwise noted.
- Output voltage amplitudes assume a 50 Ω load unless otherwise noted.
- SINE out voltage amplitude is set to 2 V_{pk-pk} with a load of 50 Ω unless otherwise noted.
- CLOCK out level set to 5 V unless otherwise noted.
- Typical specifications were determined on a small sampling of NI PXI-5404 modules.
- External calibration performed between 18 °C and 28 °C.

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Janaury 2003
323315C-01

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NATIONAL INSTRUMENTS

Output Characteristics

Table 1.

Specifications	Value	Comments
Number of outputs	1 Sine and 1 Clock—both generate same frequency simultaneously.	—

CH 0 SINE (Channel 0 Sine Wave Output, I/O Panel Connector)

Table 2.

Specifications	Value		Comments
Connector	SMB		—
Frequency Range	9 kHz to 105 MHz		—
Frequency Resolution	1.07 μHz		—
Phase Range	0° to 359.978°		—
Phase Resolution	16,384 steps including endpoints (approximately 0.022°)		—
Output Impedance	50 Ω ±4%		9 kHz to 105 MHz
Output Protection	10 V_{rms}		—
Sample Rate	300 MS/s		—
Amplitude Range	Open load	4.00 V_{pk-pk} to 2.00 V_{pk-pk}	—
	50 Ω load	2.00 V_{pk-pk} to 1.00 V_{pk-pk}	—
Amplitude Resolution	2,048 steps including endpoints Open load—Approximately 977 μV 50 Ω load—Approximately 489 μV		—
Amplitude Accuracy	±1% @ 50 kHz		—

Table 2. (Continued)

Specifications	Value		Comments
Amplitude Passband Flatness	±0.2 dB relative to the amplitude @ 50 kHz 9 kHz < f < 105 MHz		15 ºC to 50 ºC
Vertical Resolution	12 bits @ 4 V_{pk-pk} (open load) 11 bits @ 2 V_{pk-pk} (open load)		—
Bandwidth	105 MHz (0.2 dB)		15 ºC to 50 ºC
Filter	Analog—7-pole elliptical		—
SINAD	1 MHz	+51 dB	Amplitude is set to 1.8 V_{pk-pk} (~ –1 dBFS) Measured from 9 kHz to 150 MHz
	10 MHz	+48 dB	
	20 MHz	+45 dB	
	50 MHz	+42 dB	
	100 MHz	+42 dB	
SFDR	1 MHz	–55 dBc	Amplitude is set to 1.8 V_{pk-pk} (~ –1 dBFS) Measured from 9 kHz to 150 MHz Includes harmonics
	10 MHz	–54 dBc	
	20 MHz	–49 dBc	
	50 MHz	–45 dBc	
	100 MHz	–53 dBc	
THD	1 MHz	–56 dB	Amplitude is set to 1.8 V_{pk-pk} (~ –1 dBFS) Includes 2nd through the 6th harmonic
	10 MHz	–52 dB	
	20 MHz	–48 dB	
	50 MHz	–41 dB	
	100 MHz	–36 dB	
Average Noise Density	0.126 $\mu V_{rms}/\sqrt{Hz}$ –125 dBm/Hz		Integrated from 9 kHz to 150 MHz

CH 0 CLOCK (Channel 0 Clock Output, I/O Panel Connector)

Table 3.

Specifications	Value						Comments
Connector	SMB						—
Frequency Range	DC to 105 MHz						—
Frequency Resolution	1.07 μHz						—
Phase Range	0° to 359.978°						—
Phase Resolution	16,384 steps including endpoints (approximately 0.022°)						—
Output Impedance	50 Ω ±12%						DC to 105 MHz
Output Protection	+8 V to –4 V						—
Output Current	5.0 V Level		3.3 V Level		1.8 V Level		Typical Source or Sink
	120 mA		72 mA		48 mA		
Amplitude (open load)	5.0 V Level		3.3 V Level		1.8 V Level		—
	Min	Max	Min	Max	Min	Max	
V_{OL}	–0.10 V	0.40 V	–0.10 V	0.40 V	–0.10 V	0.40 V	
V_{OH}	4.00 V	5.30 V	2.60 V	3.70 V	1.40 V	2.20 V	
Amplitude (50 Ω load)	5.0 V Level		3.3 V Level		1.8 V Level		If the CH 0 CLOCK out signal is terminated into a 50 Ω load, the voltage levels are divided by two.
	Min	Max	Min	Max	Min	Max	
V_{OL}	–0.10 V	0.20 V	–0.10 V	0.20 V	–0.10 V	0.20 V	
V_{OH}	2.00 V	2.65 V	1.30 V	1.85 V	0.70 V	1.10 V	
Rise/fall time	4 ns						—
Duty Cycle Range	25% to 75%						—
Duty Cycle Accuracy	30% to 70%			±2%			Typical 1.07 μHz to 60 MHz
	25% and 75%			±3%			

PFI 0 (Programmable Function Interface, I/O Panel Connector)

Table 4.

Specifications	Value	Comments
Connector	SMB	—
Direction	Bi-directional	—
Frequency Range	DC to 20 MHz	—
As an input		
Destination for Input Signal	• PXI_Trig <0:7> (backplane connector) • REF OUT (I/O panel SMB connector) • Start Trigger	—
Input Resistance	1 kΩ ±1%	—
Input Protection	+8 V to –4 V	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
As an output		
Sources for Output Signal	• PXI_CLK10 (backplane connector) • Sample Timebase Clock (60 MHz) divided by N ($3 \le N \le 255$) • REF IN (I/O panel SMB connector) • PXI_TRIG <0:7> (backplane connector) • PXI Star Trigger (backplane connector) • CLOCK out on CH 0 (I/O panel SMB connector) • Software Trigger • Start Trigger	—
Output Impedance	50 Ω ±5%	DC to 20 MHz
Output Protection	+6 V to –1 V	—

Table 4. (Continued)

Specifications	Value		Comments
V_{OH} (minimum)	Open load	4.0 V	—
	50 Ω load	2.0 V	
V_{OL} (maximum)	Open load	0.4 V	
	50 Ω load	0.2 V	
Rise/Fall Time	4 ns		—

REF IN (Reference Input, I/O Panel Connector)

Table 5.

Specifications	Value	Comments
Connector	SMB	—
Frequency Range	1 MHz to 20 MHz (valid for PLL Reference destination) 200 kHz to 30 MHz (valid for all other destinations)	—
Destinations	• PLL Reference. Refer to Table 9 for more information. • REF OUT (I/O panel SMB connector) • PFI 0 (I/O panel SMB connector) • PXI_TRIG <0:7> (backplane connector)	—
Input Impedance	1 kΩ ±1%	—
Input Protection	12 V_{pk-pk} (sine or square wave) ± 5 VDC	—
Amplitude	300 mV_{pk-pk} to 5 V_{pk-pk} Sine or square wave	—
Input Coupling	AC	—

REF OUT (Reference Output, I/O Panel Connector)

Table 6.

Specifications	Value		Comments
Connector	SMB		—
Frequency Range	DC to 20 MHz		—
Sources	• PXI_CLK10 (backplane connector) • Sample Timebase (60 MHz) divided by N ($3 \le N \le 255$) • REF IN (I/O panel SMB connector) • PXI_TRIG <0:7> (backplane connector) • PXI Star Trigger (backplane connector) • CH 0 CLOCK out (I/O panel SMB connector) • PFI 0 (I/O panel SMB connector) • Software Trigger • Start Trigger		—
Output Impedance	50 Ω ±5%		DC to 20 MHz
Output Protection	+6 V to –1 V		—
V_{OH}	Open load	4.0 V	—
	50 Ω load	2.0 V	
V_{OL}	Open load	0.4 V	
	50 Ω load	0.2 V	
Rise/Fall Time	4 ns		—

Triggers

Table 7.

Specifications	Value	Comments
Trigger Type	Start Trigger	—
Sources	• PFI 0 (I/O panel SMB connector) • PXI_TRIG <0:7> (backplane connector • PXI Star Trigger (backplane connector) • Software (use function call) • Immediate (do not wait for a trigger). Immediate is the default setting.	—
Mode	Continuous	—
Trigger Detection	Edge (rising)	—
Pulse Width (minimum)	10 ns	—
Trigger to SINE Output Delay	250 μs	Typical

Sample Clock

Table 8.

Specifications	Value	Comments
Frequency	300 MS/s	—
Average Phase Noise Density	–112 dBc/Hz 10 MHz SINE out Offset 10 kHz ± 500 Hz	PLL Reference set to REF IN

Phase-Lock Loop (PLL)

Table 9.

Specifications	Value	Comments
PLL Reference Sources	• PXI_CLK10 (backplane connector) • REF IN (I/O panel SMB connector) • PXI_TRIG <0:7> (backplane connector) • None (default). The PLL is not used. Refer to Table 10 for more information.	—
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI PXI-5404 is solely dependent on the frequency accuracy of the PLL reference source.	—
Lock Time	200 ms	Typical
PLL Reference Frequencies	3 MHz to 20 MHz in 1 MHz increments	—
Frequency Locking Range	±50 ppm	—
PLL Reference Duty Cycles	30% to 70%	—

Internal Clock

Table 10.

Specifications	Value	Comments
Clock Source	The clock circuitry of the NI PXI-5404 can either be locked to a reference signal using the PLL or use an onboard frequency reference, specifically the Internal Clock.	—
Frequency Accuracy	±2 ppm	Typical for 15 °C to 35 °C
Frequency Temperature Coefficient	±0.3 ppm/°C	—

Multimodule Synchronization

Table 11.

Specifications	Value	Comments
Output Skew of Multiple NI PXI-5404 Modules	±1 ns when using a common PLL Reference frequency of 3, 4, 5, 6, 10, 12, 15, or 20 MHz.	—
Multimodule Output Phase Alignment	The output phase of multiple NI PXI-5404 modules can be programmatically varied after generation has started.	—

External Calibration (Factory Calibration)

Table 12.

Specifications	Value	Comments
Recommended Calibration Interval	1 year. Refer to the *NI PXI-5404 Calibration Procedure* located at `ni.com/support/calibrat/mancal`.	—
Warm-up Time	15 minutes	—

Power Requirements

Table 13.

Specifications	Value	Comments
+3.3 V Rail	1 A	SINE out, CLOCK out, and REF OUT generating maximum amplitude waveforms into 50 Ω loads
+5 V Rail	550 mA	
+12 V Rail	180 mA	
–12 V Rail	50 mA	

Software

Table 14.

Specifications	Value	Comments
Driver Software	NI-FGEN 1.6 and later provides complete IVI-compliant driver support, including calibration.	—
Application Software	Support and example programs for LabVIEW, LabWindows™/CVI™, Measurement Studio, Visual Basic, and ANSI C are included with NI-FGEN.	—
Soft Front Panel	The NI PXI-5404 is supported by the Sources Soft Front Panel 1.2 and later, which is included with NI-FGEN 1.6 and later.	—

Environment

Table 15.

Specifications	Value	Comments
Operating Temperature	0 ºC to +50 ºC	—
Storage Temperature	–20 ºC to +70 ºC	—

Physical

Table 16.

Specifications	Value	Comments
Slot	One 3U, PXI, or CompactPCI slot	—
Dimensions	10 × 16 × 2 cm (3.9 × 6.3 × 0.8 in.)	—
Weight	175 g (6.1 oz)	—
I/O Panel Connectors		
CH 0 SINE	SMB male	—
CH 0 CLOCK	SMB male	—
PFI 0	SMB male	—
REF IN	SMB male	—
REF OUT	SMB male	—
I/O Panel Indicators		
Access LED	Off—Not ready Green—Ready to be accessed by software Amber—Accessed by computer or controller	—
Active LED	Off—Disabled or in a stopped state Red—Error (PLL unlocked or software detected an error) Green—Generating a waveform Amber—Waiting for a trigger	—

Safety

The NI PXI-5404 meets the requirements of the following standards for safety and electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 3111-1, UL 61010C-1
- CAN/CSA C22.2 No. 1010.1

Note For UL and other safety certifications, refer to the product label or to `ni.com`.

Electromagnetic Compatibility

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz
Immunity	EN 61326:1997 + A2:2001, Table 1
EMC/EMI	CE, C-Tick, and FCC Part 15 (Class A) Compliant

Note For EMC compliance, you *must* operate this device with shielded cabling.

CE Compliance

This NI PXI-5404 meets the essential requirements of applicable European Directives, as amended for CE Marking, as follows:

Low-Voltage Directive (safety)	73/23/EEC
Electromagnetic Compatibility Directive (EMC)	89/336/EEC

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, click **Declaration of Conformity** at `ni.com/hardref.nsf/`. This Web site lists the DoCs by product family. Select the appropriate product family, followed by your product, and a link to the DoC appears in Adobe Acrobat format. Click the Acrobat icon to download or read the DoC.